CLAIMS

What is claimed is:

1. A self-timed scan circuit comprising:

a multiplexer for selecting either a data input or a test input in response to an internal test enable signal and for generating a multiplexed output;

a latch coupled to the multiplexer for generating a latched output in response to a next clock pulse; and

a timing control circuit for generating the internal test enable signal in response to a global test enable signal wherein the internal test enable signal is set to logic one when the global test enable signal is set to logic one and wherein the internal test enable signal is set to logic zero in response to the next clock pulse if the global test enable signal is set to logic zero before the next clock pulse.

2. The self-timed scan circuit of Claim 1 wherein the timing control circuit comprises a low power output that is set to logic one when the global test enable signal is set to logic one and wherein the low power output is identical to the latched output while the global test enable signal has a value equal to logic zero.

3. The self-timed scan circuit of Claim 1 wherein the timing control circuit comprises a latch and an OR-gate.

4. The self-timed scan circuit of Claim 1 wherein the latch is a flip-flop.

5. The self-timed scan circuit of Claim 1 wherein the global test enable signal is set to logic one asynchronously so that a logical value of the test input is latched in response to the next clock pulse.

6. A method of launch-from-shift delay testing comprising steps of:

selecting either a data input or a test input in response to an internal test enable signal for generating a multiplexed output;

latching the multiplexed output to generate a latched output in response to a next clock pulse; and

generating the internal test enable signal in response to a global test enable signal wherein the internal test enable signal is set to logic one when the global test enable signal is set to logic one and wherein the internal test enable signal is set to logic zero in response to the next clock pulse if the global test enable signal is set to logic zero before the next clock pulse.

7. The method of Claim 6 further comprising generating a low power consumption output that is set to logic one when the global test enable signal is set to logic one and is identical to the latched output while the global test enable signal has a value equal to logic zero.

8. The method of Claim 6 further comprising setting the global test enable signal to logic one asynchronously so that a logical value of the test input is latched in response to the next clock pulse.